IN THE SPECIFICATION

Please replace the first line of page 2, as follows:

~~Description~~ BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

Please insert the following subtitle between lines 4 and 5 on page 2 as follows:

DISCUSSION OF THE BACKGROUND

Please insert the following subtitle between lines 21 and 22 on page 2 as follows:

SUMMARY OF THE INVENTION

Please insert the following subtitle between lines 10 and 11 on page 5 as follows:

BRIEF DESCRIPTION OF THE DRAWINGS

Please replace the paragraph beginning at page 5, prenumbered line 17, with the following rewritten paragraph:

Fig. 2 shows a timing diagram of a first preferred embodiment according to the present invention, [[and]]

Please replace the paragraph beginning at page 5, prenumbered line 21, with the following rewritten paragraph:

Fig. 3 shows a phase locked loop for cycle synchronization according to a preferred embodiment of the present invention,

Fig. 4 shows a flowchart illustrating a method of performing a cycle synchronization between interconnected sub-networks.

Please insert the following subtitle between lines 23 and 24 on page 5 as follows:

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Please replace the paragraph beginning at page 5, prenumbered line 28, with the following rewritten paragraph:

Every IEEE 1394 node maintains cycle time information in a node. For example, Figure 1 shows a cycle master 30 that is chosen to be a reference node and a cycle master 32. This is basically a register that is incremented by a local, free-running clock of 24.576 MHz or integer multiples of that. According to the present invention this cycle time information is transmitted at regular instants via the interconnection of several sub-networks 26 and 28, in case of the example shown in Fig. 1 via the long delay bi-directional connection 24. The basic assumption of this method is that transmission of the cycle occurs at recurring time instants, preferably regular intervals, e.g. every 10 ms. Further, the exact value of that interval is not important since the exact value can be recovered from the difference of two transmitted samples of the cycle time register and the corresponding time stamps of the receiver will be sampled at the instant when the transmitted samples are received.

Please insert the following paragraphs between lines 16 and 17 on page 9 as follows:

Figure 4 is a flowchart illustrating a method for performing a cycle synchronization between interconnected sub-networks, in which a reference node connected to one of the sub-networks transmits a respective cycle type time information to cycle masters of all other sub-networks at a recurring time instance, and the cycle masters of all other sub-networks adjust their cycle time accordingly.

In the first step 401, a first time interval ($\Delta t1$, $\Delta t1'$) is determined in-between two receptions of cycle time information from the reference node 30 with an own clock, in step 403 a second time interval ($\Delta t2$, $\Delta t2'$) is determined in-between two corresponding

transmissions of cycle time information from the reference node 30 based on the received cycle time information, in step 405 the first time interval is compared to the second time interval, and in step 407 the own cycle length is adjusted according to the comparison result.

Please delete the existing Abstract at page 13, lines 3-12 and insert therefor the following new Abstract on a separate sheet as follows: